REMARKS

Claims 1-8 are pending in the application and are rejected.

Claims 1-6 Rejected Under § 103

Claims 1-6 are rejected under 35 USC § 103 as being unpatentable over Akiyama, US patent 6,009,028 (referred to as "Akiyama") in view of Todome et al., US patent 5,983,374 (referred to as "Todome"). The Office Action indicates Akiyama teaches all that is claimed except a feature of the memory that is tested (a block function by which memory cells in a block are erased en bloc and made rewritable) and the step of discontinuing the test of such block when the number of failure memory cells in a block being now tested reaches a predetermined number; that the missing memory feature was a matter of mere design choice; that Todome discloses the missing step; and that it would have been obvious to incorporate the teaching of Todome into the invention of Akiyama to reach all that is claimed.

Applicants disagree and respectfully submit the missing feature is not a matter of mere design choice and the missing step is not disclosed or suggested by Todome.

Memory Block Function

Akiyama discloses a failure self-diagnosis device for a conventional semiconductor memory. As is well known, the contents of this type of memory is volatile. In contrast to this, the memory feature recited in the claims that is not taught in Akiyama is a feature of flash memory having a block function. Such a device implements a non-volatile memory and has an internal structure of memory cells that are arranged in separate blocks and the contents of the memory cells may be erased en bloc or block-by-block en bloc, after which the contents may be rewritten.

It is known in the art that situations arise in which data cannot be written to or read from one or more cells in flash memory but these cells change under controlled conditions and begin to operate correctly. For this reason, conventional testing and diagnosis techniques like that disclosed in Akiyama are not used to test flash memory. The use of memory having "a block function by which memory cells in a block are erased en bloc and made rewritable" is not a matter of mere design choice. Changes in the processes taught in Akiyama would be needed and Akiyama neither discloses or suggests these changes.

Missing Step

Referring to the method of claim 1, the Office Action correctly indicates Akiyama does not teach the last step of the method that discontinues the testing of a block of memory under recited conditions. This step reads as follows:

> discontinuing the test of such block when the number of failure memory cells in a block being now tested reaches a predetermined number indicating repair of the memory is impossible by substitution of spare memory components.

The Office Action also indicates Todome teaches this step in its abstract and at col. 23, lns. 12-53.

Applicants respectfully disagree. Todome teaches a semiconductor test system and method in which the semiconductor device under test (DUT) has a redundant circuit (col. 1 lns. 11-13). The disclosed process includes a test phase in which the operation of the DUT is tested and it includes a remedy phase in which a "redundancy processor" determines whether if any detected faults in the DUT can be remedied (abstract, lns. 1-7). If the number of failures exceed some calculated limited, the remedy phase, not the testing phase, is terminated (abstract, lns. 17-21).

Features of this process are also described in the text of col. 23, which is cited in the Office Action, but the process may be seen more easily in Figs. 1 and 4 and col. 8 lns. 46-61, and col. 11 lns. 24-26, for example. The test phase performed by the tester 1 operates independently of the remedy phase performed by the redundancy processor 2. There is no communication from the redundancy processor 2 back to the tester 2 that can cause the test phase to stop. The redundancy processor 2 causes only the remedy phase to stop under certain conditions.

As a result, neither Akiyama nor Todome disclose or suggest the last step of claim 1. Analogous reasons apply to the last element of claim 5, which masks the test of memory cells in other blocks under specified conditions.

Claims 2-4 and 6 are dependent on claims 1 and 5, respectively, and add further limitations thereto. The Office Action does not explain where or how the prior art discloses or suggests the features of these claims; therefore, Applicants cannot do much more than state generally that these features are not taught by Akiyama or Todome.

Claims 7-8 Rejected Under § 102

Claims 7-8 are rejected under 35 USC § 102 as being anticipated by Todome.

Applicants respectfully disagree. The testing apparatus of claim 7 includes the following:

> mask control means controlling to interrupt ... the test of the block being now tested and to write, when said bad address line detection and storage means has detected a bad address line, a forced writing signal in memory cells on the detected bad address line in the test of other block or blocks to be tested thereafter, thereby to exclude such memory cells from memory cells to be tested.

As explained above, the portions of Todome cited in the Office Action refer to a remedy phase and the operation of a redundancy processor that do not affect the operation of the test or the tester. As a result, Todome does not disclose or suggest the last element of claim 7.

Claim 8 is dependent on claim 7 and adds further limitations thereto. The Office Action also does not explain where or how the prior art discloses or suggests the features of this claim; therefore, Applicants can only state generally that these features are not taught by Todome.

CONCLUSION

Applicants amend the application and request reconsideration in view of the discussion set forth above.

Respectfully submitted,

David N. Lathrop
Reg. No. 34,655
601 California St., Suite 1111
San Francisco, CA 94108-2805
Telephone: (415) 989-8080
Facsimile: (415) 989-0910

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I certify that this Response to Office Action is being deposited with the United States Postal Service on June 1, 2004 with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450..

David N. Lathrop